What is claimed is:

1. A video processor comprising:

a bit rate converter for converting an M-bit input video signal to an N-bit output video signal by retaining gray levels of the M-bit input video signal, wherein N is smaller than M; and

a gamma correction memory in which a plurality of N-bit input gray levels are mapped to a plurality of output gray levels which are distributed on a non-linear curve complementary to a non-linear curve on which gray levels of a display device are distributed,

said memory delivering one of the output gray levels when said N-bit output video signal of said bit rate converter corresponds to one of the N-bit input gray levels.

2. The video processor of claim 1, wherein said output gray levels are represented by N bits.

3. The video processor of claim 1, wherein said output gray scale values are interpolated gray levels of the input gray levels.

4. The video processor of claim 1, wherein said output gray scale values are represented by M bits.

5. The video processor of claim 1, wherein said bit rate converter comprises means for truncating lower significant bits of the M-bit video signal, representing the truncated lower significant bits by a different number of binary-1's, and distributing the binary-1's over a varying number of subsequent frames depending on the truncated lower significant bits.

6. The video processor of claim 1, wherein said bit rate converter

comprises:

a first adder for summing a binary-1 to the least significant bit position of higher N bits of the M-bit input video signal;

a first multiplexer for selecting an output of said first adder or said higher N bits in response to a first control signal;

a first frame memory for storing an output of said first multiplexer;

a second adder for summing a binary-1 to an output of the first frame memory;

a second multiplexer for selecting an output of said second adder or an output of said first frame memory in response to a second control signal;

a second frame memory for storing an output of said second multiplexer;

a third adder for summing a binary-1 to an output of the second frame memory;

a third multiplexer for selecting an output of said third adder or an output of said second frame memory in response to a third control signal;

a third frame memory for storing an output of said third multiplexer; and

control means for producing said first control signal only, said first and second control signals simultaneously, or said first, second and third control signals simultaneously, depending on the truncated lower significant bits.

7. The video processor of claim 1, wherein said bit rate converter comprises means for truncating lower significant bits of the M-bit video signal so that N bits are left in the input video signal, and dithering the N bits according to the truncated lower significant bits.

8. The video processor of claim 1, wherein said bit rate converter comprises:

an adder for summing a binary-1 to higher N bits of the M-bit input video signal;

a multiplexer for selecting an output of said adder or said higher N bits of the M-bit input video signal in response to a control signal; and

a comparator for producing said control signal by making a comparison between lower significant bits of said M-bit input video signal and a threshold value.